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L6: Entry 2 of 2 File: USPT Sep 20, 1994

DOCUMENT-IDENTIFIER: US 5349587 A
TITLE: Multiple clock rate test apparatus for testing digital systems

Abstract Text (1):
In methods and apparatus for testing a digital system, scannable memory elements of the digital system are configured in a scan mode in which the memory elements are connected to define a plurality of scan chains. A test stimulus pattern is clocked into each of the scan chains at a respective clock rate, at least two of the clock rates being different from one another. The memory elements of each scan chain are then configured in a normal operation mode in which the memory elements are interconnected by the combinational network for at least one clock cycle at a highest of the respective clock rates. The memory elements are then reconfigured in the scan mode, and a test response pattern is clocked out of each of the scan chains at its respective clock rate. The methods and apparatus are particularly useful for testing digital systems such as digital integrated circuits in which different memory elements are clocked at different rates during normal operation.

Brief Summary Text (15):
3. configuring the memory elements of each scan chain in a normal operation mode in which the memory elements are interconnected by the combinational network for at least one clock cycle at a highest of the respective clock rates;

Brief Summary Text (18):
Preferably, test stimulus patterns are clocked into all of the scan chains during overlapping time intervals, the memory elements of all scan chains are configured in normal operation mode during overlapping time intervals, and test response patterns are clocked out of all scan chains during overlapping time intervals to reduce the time required for testing. Where each scan chain consists of memory elements which are clocked at a single clock rate during normal operation, and the respective clock rate of each scan chain is made substantially equal to the clock rate during normal operation of its memory elements, the test will be reasonably representative of the digital system's operation at normal operating speed.

Brief Summary Text (19):
Another aspect of the invention provides a digital system adapted for scan testing. The digital system comprises at least one combinational network and a plurality of scannable memory elements. The memory elements are configurable in a normal operation mode in which the memory elements are interconnected by the combinational network, and are also configurable in a scan mode in which the memory elements are connected to define a plurality of scan chains. The digital system further comprises a multiple clock generator for generating multiple clock signals for clocking test patterns into and out of each of the scan chains at a respective clock rate, at least two of the clock rates being different from one another. The digital system also comprises a configuration controller for configuring the memory elements in scan mode to permit clocking of test stimulus patterns into each scan chain at its respective clock rate, for reconfiguring the memory elements in normal operation mode for at least one clock cycle at a highest of the respective clock rates, and for reconfiguring the memory elements in scan mode to permit clocking of

test response patterns out of each scan chain at its respective clock rate.

Detailed Description Text (6):
In normal scan testing of the combinational network 20, the scannable memory elements 10 are configured in scan mode by application of a suitable mode select signal MS, and a known test stimulus pattern is clocked into each scan chain 30, 40, 50 at a common test clock rate. The scannable memory elements 10 are then reconfigured in normal operation mode by changing the mode select signal MS for at least one test clock cycle so that the combinational network 20 performs logical operations on some of the data making up the test stimulus patterns and alters the data stored in some of the scannable memory elements 10. The scannable memory elements 10 are then reconfigured in scan mode by changing the mode select signal MS, and test response patterns are clocked out of each scan chain 30, 40, 50 at the common test clock rate. The test response patterns are compared with expected test response patterns to determine whether the combinational network 20 and memory elements 10 are functioning as expected.

Detailed Description Text (10):
The BIST core 60 comprises a multiple clock generator 61, a configuration controller 62, a test stimulus pattern generator 63, a test response pattern processor 64 and some control logic 65. The control logic 65 has at least one input connected to the TAP 70 and outputs connected to the multiple clock generator 61, the configuration controller 62, the test stimulus pattern generator 63 and the test response pattern processor 64 via a control bus 67. The multiple clock generator 61 has an input connected to a system clock terminal 69 of the digital system 100 and respective outputs connected to the clock inputs CK of each scan chain 30, 40, 50 via a clock bus 81. The configuration controller 62 has respective outputs connected to the mode select inputs MS of each scan chain 30, 40, 50 via a mode select bus 82. The test stimulus pattern generator 63 includes a Linear Feedback Shift Register (LFSR) having respective outputs connected to the scan inputs SI of each scan chain 30, 40, 50 via a test stimulus bus 83, and the test response pattern processor includes a LFSR having respective inputs connected to the scan outputs SO of the scan chains 30, 40, 50 via a rest response bus 84. The control logic 65 also has outputs which are connected to multiplexors 54, 55 of the boundary scan chain 50 via a boundary scan control bus 85.

Detailed Description Text (17):
To initiate scan testing, the external tester sends appropriate signals to the TAP 70 which forwards appropriate control signals to the control logic 65. The control logic 65 derives appropriate control signals for the multiple clock generator 61, the configuration controller 62 and the test stimulus pattern generator 63 which are sent via the control bus 67. The configuration controller 62 applies appropriate mode select signals to the mode select bus 82 to configure the scan chains 30, 40, 50 in scan mode. The test stimulus pattern generator 63 generates test stimulus patterns which are applied to the test stimulus bus 83 while the multiple clock generator clocks the test stimulus patterns into the scan chains 30, 40, 50 at the respective clock rates of the scan chains 30, 40, 50. When the test stimulus patterns are fully loaded into all three scan chains 30, 40, 50, the configuration controller 62 applies appropriate mode select signals to the mode select bus 82 to reconfigure the scan chains 30, 40, 50 in normal operation mode for at least one clock cycle at the respective clock rate of each scan chain 30, 40, 50. During this time interval, the test stimulus patterns are applied to the combinational network 20, changing the data stored in at least some of the memory elements. The configuration controller 62 then applies appropriate mode select signals to the mode select bus 82 to reconfigure the memory elements in scan mode, so that test response patterns are clocked out of each scan chain 30, 40, 50 during subsequent clock cycles. The test response patterns are clocked out of the scan chains 30, 40, 50 via the test response bus 84 to the test response processor 64 which compresses the test response patterns into a single test response signal. The test response processor 64 then sends the single test response signal to the

external test equipment via the TAP 70 for comparison with an expected test response signal stored in the external test equipment.

Detailed Description Text (20):
Beginning at transitions A1, A2, A3, the mode select signals MS1, MS2, MS3 are held low during respective normal mode intervals to configure the scan chains 30, 40, 50 in normal mode. Each normal mode interval corresponds to a single cycle of the corresponding clock CK1, CK2, CK3, all of the normal mode intervals overlapping for a common cycle of the highest rate clock CK1. The operation of the combinational network on the test stimulus patterns is sampled at transitions B1, B2, B3 to collect test response patterns.

Detailed Description Text (22):
Thus, the test stimulus patterns are clocked into all scan chains 30, 40, 50 during overlapping time intervals, the memory elements of all scan chains 30, 40, 50 are configured in normal operation mode during overlapping time intervals, and test response patterns are clocked out of all of the scan chains during overlapping intervals. This provides a relatively efficient test which accurately simulates the normal operation of the combinational network 20 and memory elements 10, some of which are clocked at different rates than others during normal operation. The test response patterns are collected by updating all memory elements 10 during a common period of the highest rate clock signal CK1 at transitions B1, B2, B3 while the memory elements 10 are configured in normal operation mode.

Detailed Description Text (34):
For example, the timing diagrams of FIGS. 4, 7 and 8 show mode select signals MS1, MS2, MS3 which are each held low during a single cycle of the corresponding clocks CK1, CK2, CK3. In practical embodiments, the mode select signals MS1, MS2, MS3 will generally configure each scan chain 30, 40, 50 in normal operation mode during a respective normal mode interval, all of the respective normal mode intervals overlapping in time for at least one cycle of the highest rate clock CK1. However, it is not essential that the mode select signals MS1, MS2, MS3 configure the memory elements of each scan chain 30, 40, 50 in normal operation mode for a complete clock cycle at the respective clock rate of that scan chain. For example, the mode select signals MS1, MS2, MS3 could be held low during a single common cycle of the highest rate clock as shown in dotted outline in the timing diagrams of FIGS. 4, 7 and 8, although some special precautions would be needed in dealing with memory elements employing two-edge or two-phase clocking at clock rates significantly lower than the highest clock rate.

Detailed Description Text (38):
The BIST core and TAP functions could also be implemented differently. For example, the TAP 70 need not be an IEEE 1149.1 test interface. Any suitable test interface would do. The test stimulus pattern generator 63 and the test response pattern processor 64 could be implemented in forms other than LFSRs. For example, they could be implemented as cellular automata. The multiple clock generator 61 could receive a basic clock signal from the external test equipment instead of deriving its clock signals from the system clock.

CLAIMS:

1. A method for testing a digital system comprising a plurality of scannable memory elements and at least one combinational network, the method comprising:

configuring the memory elements in a scan mode in which the memory elements are connected to define a plurality of scan chains;

clocking a test stimulus pattern into each of the scan chains at a respective clock rate, at least two of the clock rates being different from one another;

configuring the memory elements of each scan chain in a normal operation mode in which the memory elements are interconnected by the combinational network for at least one clock cycle at a highest of the respective clock rates;

configuring the memory elements in the scan mode; and

clocking a test response pattern out of each of the scan chains at its respective clock rate.

2. A method for testing a digital system comprising a plurality of scannable memory elements and at least one combinational network, the method comprising:

configuring the memory elements in a scan mode in which the memory elements are connected to define a plurality of scan chains;

clocking a test stimulus pattern into each of the scan chains at a respective clock rate during a respective scan-in interval, at least two of the clock rates being different from one another, all respective scan-in intervals overlapping in tome for a plurality of clock cycles at a highest of the respective clock rates;

configuring the memory elements of each scan chain in a normal operation mode during a respective normal mode interval, the memory elements of each scan chain being interconnected by the combinational network in the normal operation mode, all respective normal mode intervals overlapping in time for at least one clock cycle at the highest of the respective clock rates;

configuring the memory elements in the scan mode; and

clocking a test response pattern out of each of the scan chains at its respective clock rate during a respective scan-out interval, all respective scan-out intervals overlapping in time for a plurality of clock cycles at the highest of the respective clock rates.

3. A method as defined in claim 2, wherein the respective normal mode interval for each scan chain is a single clock cycle at the highest of the respective clock rates.

5. A method as defined in claim 2, wherein the respective normal mode interval for each scan chain is a single clock cycle at the respective clock rate of that scan chain.

11. A digital system comprising:

at least one combinational network;

a plurality of scannable memory elements, the memory elements being configurable in a normal operation mode in which the memory elements are interconnected by the combinational network and being configurable in a scan mode in which the memory elements are connected to define a plurality of scan chains;

a multiple clock generator for generating multiple clock signals for clocking test patterns into and out of each of the scan chains at a respective clock rate, at least tow of the clock rates being different from one another; and

a configuration controller for configuring the memory elements in scan mode to permit clocking of test stimulus patterns into each scan chain at its respective clock rate, for reconfiguring the memory elements in normal operation mode for at least one clock cycle at a highest of the respective clock rates, and for reconfiguring the memory elements in scan mode to permit clocking of test response patterns out of each scan chain at its respective clock rate.

19. A digital system as defined in claim 11, wherein:

a first memory element of a first scan chain clocked at a first clock rate supplies data via a combinational network to a second memory element of a second scan chain clocked at a second clock rate lower than the first clock rate when the memory elements are configured in normal operation mode; and

the scannable memory elements of the second scan chain are edge triggered flip-flops.

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L10: Entry 1 of 1 File: USPT Feb 1, 1994

DOCUMENT-IDENTIFIER: US 5283780 A
TITLE: Digital audio broadcasting system

Abstract Text (1):
A digital audio broadcasting system that is capable of providing a large number of high quality stereophonic channels to mobile receivers in an environment with severe multipath delay and fading. Optimum combination of frequency and time diversity to guarantee robust performance in the mobile channel, with its multipath delay and frequency-selective fading effects. The system is based upon a dynamic single channel per carrier assignment of each stereo channel to many carriers. Intersymbol interference degradations caused by multipath delay are mitigated via an adaptive equalizer in the receiver. This dynamic single channel per carrier system preserves the simplicity inherent in the single channel per carrier assignment while it incorporates the ability to address frequency-selective fading by providing substantial frequency diversity. The frequency diversity is achieved via a slow frequency hop implementation in which the assignment of a number of stereo channels to an equal number of carrier frequencies is changed periodically. The system offers the simplicity of single channel per carrier assignment of stereo channels while it achieves the powerful performance benefits of frequency diversity and adaptive equalization for the mobile channel.

Brief Summary Text (2):
The mobile channel for satellite and terrestrial digital audio broadcasting (DAB) is known to be radically affected by multipath effects that create severe degradations in signal quality that include signal fading and intersymbol interference (ISI). Fading effects on the mobile channel can be very sensitive to frequency, particularly in the urban environment. Thus, within a DAB allocated band at any instant of time, some portions of the band may be experiencing a deep fade rendering that portion of the band unusable. If a program is entirely contained in such a portion of the allocated band via single channel per carrier assignment, that program will be blacked out for the duration of the fade. The purpose of dynamic single channel per carrier system of this invention is to periodically change single channel per carrier assignments in a dynamic way such that all programs in an allocated DAB frequency band uniformly occupy the entire frequency band. In so doing, all programs are protected against frequency-selective fades in the allocated band. Moreover, by providing an optimum combination of frequency and time diversity, the dynamic single channel per carrier system ensures that up to 20% or more of the allocated band can be in deep fade without affecting the sound quality of any of the programs. Thus, the dynamic single channel per carrier system of program allocation and coding provides robust digital audio broadcasting performance in the mobile channel environment with severe frequency-selective fading.

Brief Summary Text (12):
Time diversity requires an orderly scrambling of the data symbols prior to transmission and the restoration of the order at the output of the receiver. The goal of the orderly scrambling and descrambling is to transform a burst of errors that occur on the propagation channel during a deep fade into random errors at the